SEM VII EComE

Syllabus

Course Name: Internet of Things **[2:0:2=3]**

Course Content

What is IoT and Why is IoT, Cool applications of IoT. Potential and challenges, IoT architecture. Sensors: sensor terminology, sensor dynamics and specifications. Linearization and error, noise, picking a sensor. Circuits: overview of circuits used in IoT, battery current, and wireless links, digital computing and analog to digital interfaces. Embedded systems: internet connectivity and MGC architecture, Cortex M and BLE. Typical cost and computing an energy budget. TCP/IP model. Network protocols and standards for internet of things. HTML, CSS, JavaScript, NodeJS, Express JS, Mongo DB. HTTP, MQTT, and CoAP protocol. HTTP Webserver, MQTT client and subscriber. Web socket programming. IoT case study e.g. voice activated control, home automation, industrial automation, smart grid, smart cities etc. Setup open source IoT platform

Course Outcomes

CO1: Understand IoT architecture, protocols needed for communication

CO2: Analyze various sensors and there dynamics

CO3: Design circuits and embedded hardware used for IoT applications

Text Book:

1) IoT fundamentals Networking technologies, protocols, and used cases by David hanes, Cisco press
2) Computer Network by Tennenbaum
3) Smart Internet of Things by Agus kurvian

Course Name: Advance Computer Architecture **[3:0:0=3]**

Course Content

Metrics for computer performance: clock rate, MIPS, CPI Strength and weakness of performance metrics role of Amdalh's in computer performance Hierarchical memory system, main, cache and auxiliary memory, I/O subsystem, Average and Worst-case access time, multi-level cache memory, Split Cache, Cache Consistency. Classification of computer architecture: SIMD, MIMD, SISD and MISD Processing unit design: Data path implementation, Microprogrammed execution.

Principles of pipelining and vector processing: Pipelining, Instruction and Arithmetic Pipelines, Principles of Designing Pipelined Processor, Instruction pipelining and parallel processing. Instruction level parallelism: VLIW, Vector processor, Multithreaded processor, Superscalar architecture branch prediction Prefetching Speculative execution Vector Processing Requirements. Structure and Algorithms for array processors: SIMD Array Processors, SIMD Interconnection Networks, Parallel Algorithms for array Processors, Programming, Performance Evaluation and Compiler Transformations for parallel computers. Associative Array Processing. Multiprocessor architecture and programming: Inter processor Communication Mechanisms, System Deadlocks and Protection, Multiprocessor Scheduling Strategies, Parallel Algorithm for Multiprocessor. Multiprocessor and Multi Computer architectures. Cache coherence problem. On-chip interconnection networks: Bus-based interconnects; on-chip packet switched networks. Special-purpose architectures. Converging approaches to computer design.

Course Outcomes

CO1: Understand different processor architectures, system-level design processes, components and operation of a memory hierarchy

CO2: Predict the challenges of realizing different kinds of parallelism (such as instruction, data, thread, core level) and leverage them for performance advancement.

CO3: Apply the concept of memory hierarchy for efficient memory design and virtual memory to overcome the memory wall.

Textbook:

1) John L. Hennessey and David A. Patterson, "Computer Architecture A Quantitative Approach", Morgan Kaufmann/ Elsevier, Fifth Edition, 2012.
2) Kai Hwang and Faye Briggs, "Computer Architecture and Parallel Processing", Mc Graw-Hill International Edition, 2000.